APPLICATION

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TITLE: IMPROVED INTEGRATED CHIP PACKAGE HAVING INTERMEDIATE SUBSTRATE

APPLICANT: SEHAT SUTARDJA

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IMPROVED INTEGRATED CHIP PACKAGE HAVING INTERMEDIATE SUBSTRATE

TECHNICAL FIELD

[0001] The present invention relates to integrated circuit packaging, and more particularly to packaging of flip chip semiconductors.

BACKGROUND

[0002] The drive to higher semiconductor device densities places increased demands on the packaging for these devices to remove heat generated from dissipated power in the device. One low cost packaging technique that has been used device having lower densities is plastic ball gate array (PBGA). In a PBGA thermal vias on the underside of the encapsulated die provide a thermal path for the thermal energy to the circuit board. Typically, a PBGA is limited to dissipating less than approximately 2.5 watts. The low power dissipation capability of a PBGA is quickly being exceeded by the power requirements of today's high density devices. In addition, routing the thermal energy into the circuit board limits the number of semiconductor devices that can be mounted on the circuit board.

[0003] Flip chip ball gate array (FCBGA) is a packaging technique that is capable of supporting semiconductor devices

that dissipate more than 20 watts of power. In a FCBGA, the semiconductor device or integrated circuit chip is connected to a package substrate via solder balls. The package substrate is coupled to the circuit board through solder balls on the underside of the package. To connect the pads of the device or chip to the solder balls, the package substrate typically uses a build-up construction to permit the use of extremely fine pitch wiring for the interconnection. Although a FCBGA provides a packaging solution for high dissipation devices, the cost of a FCBGA is very high due to the need for a substrate having a build-up construction.

SUMMARY

[0004] The present integrated chip package provides a low cost package that is suitable for high density semiconductors that have high power dissipation. The integrated chip package includes at least one semiconductor chip having a first surface and a second surface. The first surface of the semiconductor chip is electrically coupled to an intermediate substrate via conductive bumps. The intermediate substrate is also electrically coupled to a package substrate via a plurality of bonding wires. The second surface of the semiconductor chip is thermally coupled to a heat sink to increase the power dissipation capacity of the integrated chip package.

[0005] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0006] Figure 1 shows a first embodiment of an integrated chip package in accordance with the principles of the invention;

[0007] Figure 2 shows a shows a second embodiment of an integrated chip package in accordance with the principles of the invention;

[0008] Figure 3A shows an interface of an intermediate substrate to a semiconductor chip;

[0009] Figure 3B shows an equivalent circuit diagram of an interface of an intermediate substrate to a semiconductor chip;

[0010] Figure 4 shows an embodiment of an intermediate substrate; and

[0011] Figure 5 shows a method of manufacturing an integrated chip package in accordance with the principles of the invention.

[0012] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0013] Referring to Figure 1, a first embodiment of an integrated chip package 10 in accordance with the principles of the invention is shown. The integrated chip package 10 is a modified FCBGA that can advantageously dissipate approximately the same amount of heat as a flip chip package at a much lower cost. In addition, the thermal path of the integrated chip package 10 extends away from the circuit board to reduce the heat load on the circuit board.

[0014] The integrated chip package 10 includes a semiconductor chip 12 configured for flip chip mounting that is attached to an intermediate substrate 14. A first surface 16 of the semiconductor chip 12 is electrically connected to the intermediate substrate 14 via conductive bumps 18. The conductive bumps 18 may be formed from any electrically conductive material such as Pb/Sn solder, Au, Ag, alloys of Au and Ag, and metallic coated polymeric studs. In addition, an epoxy 13 or other suitable material formed between the conductive bumps 18 may be used as an embedding material for the conductive bumps 18 to provide mechanical support and moisture protection. The semiconductor chip 12 may be attached to the intermediate substrate 14 using any flip chip compatible bonding

method such as thermocompression, soldering, encapsulation, and adhesives.

[0015] The other surface 20 of the semiconductor chip 12 is attached to a heat sink 22 for coupling heat away from the semiconductor chip 12. The heat sink 22 may be made of any thermally conductive material such as copper and thermally conductive plastic. The semiconductor chip 12 may be attached to the heat sink 22 by any attachment item 24 that does not thermally isolate the semiconductor chip 12 such as adhesive, solder, and press-fitting by applying a mechanical force to the first surface of the semiconductor chip 12 or the intermediate substrate 14. For example, a thermally conductive epoxy may be used as the attachment item 24.

[0016] The intermediate substrate 14 is electrically connected to conductors on a package substrate 26 via several bonding wires 28. The intermediate substrate 14 converts flip chip mounting of the semiconductor chip 12 into wire bond mounting to combine and exceed the advantages of FCBGA and PBGA. Similar to FCBGA, the integrated chip package 10 provides a low resistance thermal path for heat generated in the semiconductor chip 12 so that power dissipation exceeding 20 watts may be accommodated. In addition, the thermal path of the integrated chip package 10 extends to the heat sink 22, away from the

package substrate 26, thereby reducing the heat load of the circuit board or circuit substrate to which the integrated chip package 10 is connected. Also, the integrated chip package may employ a substrate that is as inexpensive as substrates used for PBGA packages. Additionally, using the intermediate substrate 14 reduces the wiring pitch requirements on bonding wire equipment used for attaching the bonding wires 28.

[0017] Referring to Figures 1 and 2, the intermediate substrate 14 may be made from any substrate material such as normal silicon wafer (either low or high quality), polysilicon, and glass. Circuit planes such as power planes, ground planes, and interconnect planes may be added to the intermediate substrate 14. The process technology used for the circuit planes is not limited to the technology used for the semiconductor chip 12. Instead, other process technologies including lower cost technologies such as 1 micron technology may be employed to reduce the cost of the package 10. The circuit planes may provide interconnect within the semiconductor chip 12 as well as to the package substrate 26 through the bonding wires 28. Including circuit planes in the intermediate substrate 14 may reduce the requirement for expensive power and ground grids on the semiconductor chip. For example at 0.13 um, each layer of metalization costs about 10 times more than the

cost of providing the same function on the intermediate substrate 14. Moreover, the semiconductor chip 12 may employ distributed power and ground conductive bumps to achieve substantially lower impedance. Decoupling capacitors 32 may be included on the intermediate substrate to provide local filtering of power and ground signals. Providing local filtering is particularly advantageous in view of the high DC and AC currents that may flow between the intermediate substrate 18 and the semiconductor chip 12. For example, in a 20 watt device operated with 1 volt supply voltage, the DC current is 20 amps with an AC current that may be 150 amps. In view of such high magnitude AC currents, providing local filtering with low inductance paths is crucial to maintain a relatively constant supply voltage. The decoupling capacitors 32 may include one or more small capacitors as well as a single large parallel plate capacitor 31 covering the whole substrate. The values of the capacitors may be controlled by varying the thickness and area of the dielectric. For example, the value of a parallel plate capacitor 31 may be controlled by varying the thickness of a layer of silicon between the metallized plates. Additional capacitor materials may be used that otherwise are generally not used in advanced wafer fabrication because of concerns with contaminating the wafer. Examples of capacitor materials

include standard oxides and nitride oxides. In addition, trench capacitors 33 may be formed on the intermediate substrate 14. Trench capacitors advantageously provide higher volumetric efficiency than parallel plate capacitors. Practically one entire side of the intermediate substrate 14 may be used for decoupling capacitors 32, as well as portions of the other side of the intermediate substrate 14.

[0018] The package substrate 26 may be made of any substrate material suitable for ball grid array mounting to a device such as a circuit board or substrate. Additionally, a support layer 25 such as an epoxy or other suitable material may be inserted between the intermediate substrate 18 and the package 26 to provide addition mechanical support.

[0019] Shown in Figure 3A is an expanded view of the interface of the intermediate substrate 14 to the semiconductor chip 12 via the conductive bumps 18. The intermediate substrate 14 may include several metalization layers 27 separated by insulation layers 28. The conductive bumps 18 are aligned with the metalization layers 27 to provide an electrical connection between the intermediate substrate 14 and the semiconductor chip 12. The metalization layers 27 and insulation layers 28 may be configured to form local decoupling capacitors.

[0020] Shown in Figure 3B is a circuit diagram illustrating the interface shown in Figure 3A. Capacitors 29a and 29b represent the capacitance formed between the metalization layers 27.

[0021] Shown in Figure 4 is a second embodiment of an integrated chip package 40 in accordance with the principles of the invention is shown. The integrated chip package 40 is similar in function to the integrated chip package 10, with corresponding elements numbered in the range 40-60, except that the integrated chip package 40 includes several semiconductor chips 42a and 42b attached to each intermediate substrate 44 to form a multichip module (MCM). In this embodiment, semiconductor chip 42a may be a logic circuit and semiconductor chip 42b may be a power device. Any combination of semiconductor chips 42 may be used including all logic devices, all power devices, or a mix of logic devices and power devices. In addition, the quantity of semiconductor chips that may be mounted within the integrated chip package 40 is not limited to merely two. The intermediate substrate 44 may be used to provide interconnects within the semiconductor chips 42a and 42b, among the semiconductor chips 42a and 42b, and from the semiconductor chips 42a and 42b to the conductive bumps 60. Thousands of bonding wires may be provided between the

intermediate substrate 14 and the package substrate 56 for very low cost. Since many of the interconnects between the semiconductor chips 44 are made on the intermediate substrate 44, the quantity of bonding wire interconnects within the integrated chip package 40 may be significantly reduced. This is particularly advantageous with system on a package (SOP), where the power dissipation of devices within the package 40 exceeds 20 watts.

[0022] Shown in Figure 5 is a method of manufacturing an integrated chip package 10 in accordance with the principles of the invention. At block 70 a semiconductor chip to be packaged is provided. The semiconductor chip is flip chip mounted to an intermediate substrate, block 72. The semiconductor chip is then thermally attached to a heat sink, block 74. At block 76, bonding wires are connected between the intermediate substrate and a package substrate. At block 78, conductors that are suitable for ball gate array mounting are formed on the package substrate.

[0023] A number of embodiments of the invention have been described. It is expressly intended that the foregoing description and accompanying drawings are illustrative of preferred embodiments only, not limiting, and that the true spirit and scope of the present invention will be determined by

reference to the appended claims and their legal equivalent. It will be equally apparent and is contemplated that various modifications and/or changes may be made in the illustrated embodiments without departure from the spirit and scope of the invention. For example, the steps of the method of manufacturing may be performed in numerous different sequences. Accordingly, other embodiments are within the scope of the following claims.